Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 13 are presently pending in the application. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

In item 3 of the above-identified Office Action, claims 1 - 5, 7 - 10, 12 and 13 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by U. S. Patent No. 6,477,674 to Bates et al ("**BATES**").

In item 4 of the Office Action, claim 6 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BATES** in view of U. S. Patent No. 6,704,897 to Takagi ("**TAKAGI**"). In item 5 of the Office Action, claim 11 was rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **BATES** in view of U. S. Patent No. 5,751,151 to Levy et al ("**LEVY**").

Applicant respectfully traverses the above rejections.

More particularly, claim 1 recites, among other limitations:

> first and second equally sized groups of interface circuits, **wherein each interface circuit of said first group is assigned exactly one interface circuit of said second group;** [emphasis added by Applicant]

Claim 7 incorporates therein all limitations of claim 1, and thus, likewise, recites the above limitation. As such, all of Applicant's claims require, among other things, **a 1:1 correspondence between interface circuits of a first group and interface circuits of a second group** (i.e., each interface circuit of the first group being assigned to exactly one interface circuit of the second group).

Applicant's claims 1 and 7 additionally recite, among other limitations:

> **a respective electrical connection of the interface circuits of said first and second groups to outside of the semiconductor module, for enabling a self-test;** [emphasis added by Applicant]

As such, Applicant's claimed invention requires, among other things, **electrical connections to the first and second interface circuits, for enabling a self-test.**

Applicant believes that the **BATES** reference fails to teach or suggest: 1) Applicant's particularly claimed 1:1 correspondence between the interface circuits of the first and second groups; and 2) the electrical connections from the interface circuits for self-testing.

More particularly, **BATES** discloses a method and apparatus for conducting input/output loopback tests using a local pattern generator and delay elements. **BATES** discloses an integrated circuit including a plurality of I/O buffers, each of which includes an I/O test circuit that generates test pattern signals whenever the integrated circuit is operating in a loopback test mode. See the Abstract of **BATES**. Pages 2 - 3 of the Office Action state, in part:

> The Applicant argues on pages 9 and 10 "However, BATES does not particularly disclose much about these 'other IC 100 devices'. For example, BATES does not particularly disclose whether these 'other IC 100 devices' are arranged in a second group of input/output buffers or if such a 'second group' comprises the same number of input/output buffers as the first group . . . .". In response to Applicant's argument the Examiner would like to refer the Applicant back to Figure 5, which is a block diagram of one embodiment of an integrated circuit (IC) 500 that includes input/output (I/O) buffers 100(1)-100(n). I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices. The "other IC 100 devices" Bates is referring to, as **interpreted by the Examiner**, is a duplication of IC 500 that includes other groups of input/output (I/O) buffers 100(1)-100(n), which qualifies the "other IC 100 devices" as the second group. Bates continues to teach that a data block includes sixteen (16) I/O buffers 100. However, in other embodiments, a data block may include other multiples (e.g., 2, 4, 8, 12, 18, 32, 40, 64, etc.) of I/O buffers 100. (Col. 4, 11.28 - 37). **It stands to reason to one skilled in the art that the I/O buffers 100 (i.e. as well as other IC 100 devices) are groups that are duplicated and therefore, comprises the same number of input/output buffers as the first group.** In light of the arguments presented above, **the Examiner's only conclusion** is that Bates substantially teaches "first and second equally sized groups of interface circuits, wherein each interface circuit of said first group is

> assigned exactly one interface circuit of said second group;" and "a first circuit connected to said first group and serving to generate test signals to be multiplexed in and output via said interface circuits of said first group; a second circuit connected to said second group for receiving and processing test signals received via said interface circuits of said second group;" [emphasis added by Applicant]

Applicant respectfully traverses the above statement from the Office Action.

**BATES** does not explicitly state or show that "other IC 100 devices" are I/O devices in equal number to and/or correspond in a 1:1 relationship with the I/O devices 100(1) - 100(n) shown in Fig. 5. This is supported by the above quoted section of the Office Action. Further, in countering Applicant's arguments to this effect, the Office Action uses such phrases as "**as interpreted by the Examiner**", "**It stands to reason to one skilled in the art that**", and "**the Examiner's only conclusion**", which implies that the standard being used to apply **BATES** to Applicant's claims is one of **obviousness**. However, Applicant notes that Applicant's independent claims 1 and 7, including the above limitations, as well as other claims, were rejected under 35 U.S.C. § **102(e)**, which section regards alleged **anticipation** by a reference. As stated in MPEP § 706.02:

**IV. DISTINCTION BETWEEN 35 U.S.C. 102 AND 103**

> The distinction between rejections based on **35 U.S.C. 102** and those based on **35 U.S.C. 103** should be kept in mind. Under the former, the claim is anticipated by the reference. **No question of obviousness is present.** In other words, for anticipation under **35 U.S.C. 102**, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. Whereas, in a rejection based on **35 U.S.C. 103**, the reference teachings must somehow be modified in order to meet the claims. The modification must be one which would have been obvious to one of ordinary skill in the art at the time the invention was made. See **MPEP § 2131 - § 2146** for guidance on patentability determinations under **35 U.S.C. 102** and **103**. [emphasis added by Applicant]

As such, if, indeed, a standard of **obviousness** is being applied against Applicant's claims, it is respectfully requested that the present rejection be withdrawn, and a new rejection based on 35 U.S.C. § 103(a), be issued in its place.

Further, as stated above, Applicant maintains its belief that the **BATES** reference fails to teach or suggest, among other limitations of Applicant's claims, the particularly claimed 1:1 correspondence between the interface circuits of the first and second groups. Page 5 of the Office Action again points to col. 4 of **BATES**, lines 28 - 36, as allegedly disclosing Applicant's particularly claimed first and second equally sized groups of interface circuits. Applicant respectfully disagrees. Col. 4 of **BATES**, lines 28 - 36, states:

> FIG. 5 is a block diagram of one embodiment of an integrated circuit (IC) 500. IC 500 includes

> input/output (I/O) buffers 100(1)-100(n). I/O buffers 100(1)-100(n) make up a data block of I/O circuitry for transmitting to and receiving data from other IC 100 devices.

Col. 4, lines 32 - 36 of **BATES** identifies the number of buffers illustrated in Figure 5.

However, Applicant maintains that Fig. 5 of **BATES** only discloses one single plurality of buffers 100(1) - 100(n). More particularly, Applicant maintains that **BATES** fails to teach or suggest that <u>each</u> of the buffers 100(1) - 100(n) of Fig. 5 of **BATES** is assigned to <u>one</u> respective corresponding interface circuit or buffer of a second, equally sized group of interface circuits.

Col. 4 of **BATES**, lines 50 - 52 merely discloses that, in general, input/output buffers 100 maybe connected to one another. However, this disclosure in **BATES refers to normal operation mode but not to test mode.** Furthermore, in **BATES'** normal mode of operation, input/output buffers of the integrated circuit usually are connected to input/output buffers <u>of another integrated circuit,</u> **but not to further input/output buffers of the same integrated circuit.** In normal operation of a device, when plural integrated circuits are provided and connected to one another within a larger electronic component, **input/output buffers of a first**

integrated circuit will not be connected to further input/output buffers of the same integrated circuit chip but only to input/output buffers of the second (perhaps identical) integrated circuit chip. Otherwise, the input/output buffers would not to be called "input/output" buffers, because, in normal operation mode, any "input/output" buffers are forwarding signals either leaving or arriving at the chip.

Further, the Examiner's "**conclusion**", made in the Office Action, is contradictory to the technical teachings of **BATES**. Fig. 1 of **BATES** illustrates one single buffer 100, including a test circuit 110 for test pattern generation, an output driver (comprising elements 115, 120, 125 and 130) and an input receiver (comprising elements 145 and 150). In **BATES'** normal operation mode, signals may be forwarded from the core (See Fig. 1 of **BATES**, upper left corner) via the output driver and the input/output pad 135 to another chip. Alternatively, signals arriving at the chip, via pad 135 of Fig. 1 of **BATES**, may be sent via the input receiver to the core (See Fig. 1 of **BATES**, bottom left corner).

According to **BATES**, the input/output buffers 100 each include a test circuit 110 for performing a self-test of the respective input/output buffer. This test is referred to as the "I/O loopback test" in **BATES**, col. 1, line 33, col. 2,

line 47, column 3, lines 34 and 48 and column 6, line 25. In **BATES'**, a respective buffer 100 is tested during the I/O loopback self-test to determine whether the respective buffer is defective. As such, the loopback self-test of **BATES** performs a test **within, and only within, the respective buffer** electrical path including elements 115, 120, 125, 130, 145, 150, 110 **to test if the respective buffer is operating properly.** In particular, in the test mode of **BATES** no test signals are leaving the respective buffer 100 under test, via the input/output pad 135 (Fig. 1 of **BATES**) **since only the internal electronic components of the respective buffer 100 are tested.**

Fig. 2 of **BATES** illustrates a detailed view of the I/O test circuit 110 which serves to generate the test pattern signals. **BATES'** test circuit 110 includes a test pattern generator 210, an output line connected to MUX 115 of the buffer 100 (compare Figs. 1 and 2 of **BATES**) and an input line for receiving input signals incoming from amplifier 145 (compare Figs. 1 and 2 of **BATES**; and col. 3, lines 62 - 64 of **BATES**). Further, the test circuit 110 illustrated in Fig. 2 OF **BATES** (and provided in each input/output buffer 100, as illustrated in Fig. 1 of **BATES**) includes a stage 215. Col. 3 of **BATES**, lines 60 - 64, states:

According to one embodiment, stage unit 215 provides a

> one cycle delay for the test pattern signals before they are transmitted to compare unit 220 be compared with test signals received from amp 145.

As such, the stage unit 215 of **BATES** serves to directly connect the generated test pattern signal to the compare unit 220. See **BATES**, Fig. 2. By this way, in **BATES**, a duplicated test pattern signal is provided for comparison with the signal received from amplifier 145. See **BATES**, col. 5, lines 65 - 67.

In reviewing Fig. 1 and 2 of **BATES** in context with one another, it becomes apparent that **each buffer 100 includes a test circuit 110 generating a test signal**, which, in the form of a first **duplicate** signal, is passed across elements 115, 120, 125, 130, 145, 150 **within the respective buffer 100**, before again arriving in the test circuit 110 for comparison in the compare unit 220. The second duplicate signal is sent directly within the test circuit 110 to the stage 215 and from the stage 215 to the compare unit 220. Note that **each** buffer 100 shown in Figs. 1 and 5 of **BATES**, must include its own, **respective test circuit** 110, which **only** serves to test the **respective** individual buffer 100.

When this self-test of the respective buffer is performed in **BATES**, **no electrical connection to any other second corresponding input/output buffer 100 is made, at all**. In

particular, during the self-test mode for a particular buffer in BATES, no test signal is leaving the respective buffer 100 via the input/output pad 135 or being sent to an input/output pad 135 of a second respective input/output buffer.

In BATES, plural buffers may be connected to one another, but only in normal operation mode and only to buffers of another chip. In the test mode of BATES, however, the closed loop for the test pattern signal extends only within the respective buffer 100, starting from the test circuit 110, and arriving back at the same test circuit 110.

Col. 7 of BATES, lines 1 - 3 explicitly discloses:

> A particular I/O buffer 100(x) will be considered to have failed the test if the expected test data is not received at latch 230.

As such, the loopback self-test of BATES does not involve communication with any second buffer of any second group.

In particular, in BATES, when the self-tests are performed, none of the buffers 100 are assigned to any further second buffer. In BATES, there is no second plurality of buffers which, during the self-test, would be assigned to the buffers of the first group. See also, col. 6 of BATES, lines 27 - 29 ("If all of the test pattern signals have been issued (e.g., a

sufficient number of test cycles have been run), latch 230 may be examined to determine whether a defect was detected in I/O buffer 100 during the transmission of previous test signals, process block 445").

Accordingly, **BATES** discloses a loopback test that directly detects a defect in a respective tested buffer 100, but neither teaches, nor suggests, connecting the respective tested buffer 100 to a second buffer assigned thereto. The direct testing of each buffer 100 of **BATES** is only possible because the loopback self-test signal at the output of the driver 130 (Fig. 1 of **BATES**) is sent directly to the amplifier (145 of Fig. 1 of **BATES**, rather than to pad 135) so as to constitute a buffer-internal self-test loop. Otherwise, were each buffer 100 connected to or assigned to a second respective buffer (i.e, of a second group as claimed by Applicant) it would not be possible to assign the defect to one particular buffer. As such, it is clear that the buffers 100(1) - 100(n) of Fig. 5 of **BATES**, are not connected to a second group of buffers 100(1) - 100(n) (not illustrated in **BATES**) during the loopback self-test of the buffers 100(1) - 100(n).

Further, since each of the buffers 100 of **BATES** includes its own, respective test circuit 110 (as shown in Fig. 1 of **BATES**)

having a test pattern generator 110 and a compare unit 220, as well as a stage 215, **each buffer 100 is capable of testing itself without the need to be connected to any second buffer**. Accordingly, it is not correct to interpret or conclude (as done on pages 2 and 3 of the Office Action) that two respective self-testing buffers 100 would be assigned to one another. If this assumption were correct in the system disclosed in **BATES**, it would be questionable how the second buffer 100 of **BATES** would process the test signals received from the, first buffer.

Actually, however, each test circuit 110 of any respective buffer 100 of **BATES**, can only compare those test signal duplicates (originated and received back) which are generated by the same test circuit 110 (i.e., the test circuit of the buffer 100 containing the test circuit 110). Any assumption that two respective buffers 100 of **BATES**, would cooperate with one another is in direct conflict with the explicit teachings of **BATES**, that each buffer 100 is testing itself (i.e. loopback "self-test"). As such, it can be seen that **BATES** fails to teach or suggest the assignment of second buffers of a second group to first buffers of a first group.

As such, **BATES** fails to teach or suggest, among other limitations of Applicant's claims 1 and 7: 1) that there is

any 1:1-correspondence between buffers of a first group and buffers of a second group; and 2) that there is an electrical connection of the interface circuits to outside for enabling a self-test. In contrast to Applicant's particularly claimed invention, **BATES** discloses, **that the electrical connection to outside** (i.e., the input/output pad 135 of Fig. 1 of **BATES**) **is unused when performing the self-test,** since **BATES** teaches that the self-test signals are sent from the driver 130 directly to the amplifier 145, in order to test the output driver (elements 115 to 130) and the input receiver (elements 145 and 150) of the buffer 100.

Further, for the reasons discussed thoroughly above, it can be seen that **BATES** additionally fails to teach or suggest, a self-test method, as in Applicant's claim 7, including, among other limitations:

> **receiving** the test signals **via** the second group of interface circuits; [emphasis added by Applicant]

A review of **BATES** makes clear that the test signals generated by the test circuit 110 of each buffer 100 **remain within the respective buffer 100.**

The **TAKAGI** and **LEVY** references, cited in the Office Action in combination with **BATES**, against certain of Applicant's

dependent claims, do not cure the deficiencies of **BATES**, discussed above.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 7. Claims 1 and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 7.

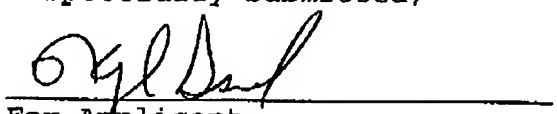
In view of the foregoing, reconsideration and allowance of claims 1 - 13 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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